WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a pair of a first power wiring and a second power wiring, the pairs being arranged in one direction, wherein a first region between the first power wiring and the second power wiring;

fundamental circuit units constituted by combining one or more PMOS transistors and one or more NMOS transistors, the fundamental circuit units being arranged along with the first power wiring and the second power wiring;

logic circuit units constituted by a plurality of the fundamental circuit units;

functional circuit units constituted by a plurality of the logic circuit units, the functional circuit units being connected each other; wherein

at least one part of the PMOS transistors and that of the NMOS transistors are arranged below the first power wiring and the second power wiring; and

unit connection wirings to connect between the fundamental circuit units or to connect between the logic circuit units, of which terminals terminate at the functional circuit units are arranged on second regions that are other than the first region, in case the unit connection wirings are constituted by a layer that is same as a wiring layer that constitutes the first power wiring and the second power wiring or by wiring layers that are under the wiring layer of the first and second power wirings.

2. A semiconductor integrated circuit device according to claim 1, wherein PMOS transistors and an N-type well region that surrounds the PMOS transistors are arranged under the first power wiring along the first power wiring, and NMOS transistors and a P-type well region that surrounds the NMOS transistors are arranged under the second power wiring along the second power wiring.

3. A semiconductor integrated circuit device according to claim 1, wherein the unit connection wirings are arranged on regions that are parts of the

second regions and outside of the PMOS transistors and the NMOS transistors.

4. A semiconductor integrated circuit device according to claim 3, wherein the unit connection wirings are arranged on a part of the second region that is at the first power wiring side, and the PMOS transistors are included in the first power wiring.

5. A semiconductor integrated circuit device according to claim 3, wherein the unit connection wirings are arranged on a part of the second region that is at the second power wiring side, and the NMOS transistors are included in the second power wiring.

6. A semiconductor integrated circuit device according to claim 4, wherein the PMOS transistors are arranged in a manner that their edge at a side of the unit connection wirings is aligned with an edge at a side of the unit connection wirings for the first power wiring.

7. A semiconductor integrated circuit device according to claim 5, wherein the PMOS transistors are arranged in a manner that their edge at a side of the unit connection wirings is aligned with an edge at a side of the unit connection wirings for the first power wiring.

8. A semiconductor integrated circuit device according to claim 4, wherein the NMOS transistors are arranged in a manner that their edge at a side of the unit connection wirings is aligned with an edge at a side of the unit connection wirings for the second power wiring.

9. A semiconductor integrated circuit device according to claim 5, wherein the NMOS transistors are arranged in a manner that their edge at a side of the unit connection wirings is aligned with an edge at a side of the

unit connection wirings for the second power wiring.

10. A semiconductor integrated circuit device according to claim 4, wherein in case the fundamental circuit units constitute a first NAND gate, the number of gates for the NMOS transistors is same as that for the PMOS transistors in a layout pattern of the first NAND gate.

11. A semiconductor integrated circuit device according to claim 4, wherein in case the fundamental circuit units constitute a first NOR gate, the number of gates for the PMOS transistors is same or larger than that for the NMOS transistors in a layout pattern of the first NOR gate.

12. A semiconductor integrated circuit device according to claim 5, wherein in case the fundamental circuit units constitute a second NAND gate, the number of gates for the NMOS transistors is same or larger than that for the PMOS transistors in a layout pattern of the second NAND gate.

13. A semiconductor integrated circuit device according to claim 5, wherein in case the fundamental circuit units constitute a second NOR gate, the number of gates for the NMOS transistors is same as that for the PMOS transistors in a layout pattern of the second NOR gate.

14. A semiconductor integrated circuit device according to claim 4, wherein two pairs of the functional circuit unit groups arranged with multi-staged structure on demand are arranged in a mirror reverse manner with reference to an edge opposite to an arrangement region of the unit connection wirings.

15. A semiconductor integrated circuit device according to claim 5, wherein two pairs of the functional circuit unit groups arranged with multi-staged structure on demand are arranged in a mirror reverse manner with reference

to an edge opposite to an arrangement region of the unit connection wirings.

16. A semiconductor integrated circuit device according to claim 14, wherein in the two pairs of the functional circuit unit groups arranged in a mirror reverse manner, a well region that surrounds same-conductive type transistors arranged in a mirror reverse manner is shared by the two pairs of the functional circuit unit groups.

17. A semiconductor integrated circuit device according to claim 15, wherein in the two pairs of the functional circuit unit groups arranged in a mirror reverse manner, a well region that surrounds same-conductive type transistors arranged in a mirror reverse manner is shared by the two pairs of the functional circuit unit groups.

18. A semiconductor integrated circuit device according to claim 16, wherein a contact region for applying bias to the well region is shared by the two pairs of the functional circuit unit groups.

19. A semiconductor integrated circuit device according to claim 17, wherein a contact region for applying bias to the well region is shared by the two pairs of the functional circuit unit groups.